

# EUROPEAN PATENT OFFICE

## Patent Abstracts of Japan

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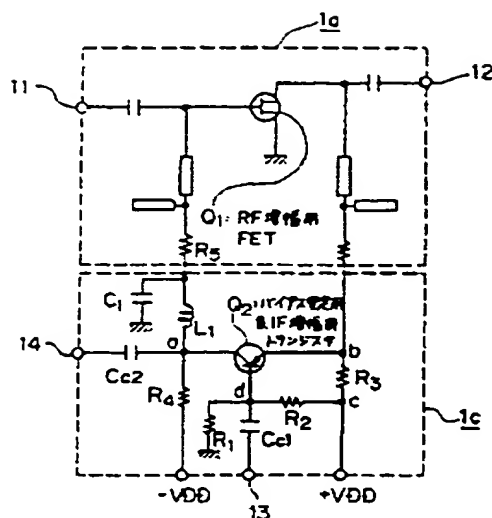
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APPLICATION NUMBER : 63141023

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TITLE : AMPLIFIER CIRCUIT FOR BS  
CONVERTER



ABSTRACT : PURPOSE: To attain small size and to reduce the cost with a few component number by using a bias stabilizing transistor (TR) suppressing the fluctuation of a drain current of a high frequency (RF) amplification FET so as to constitute an intermediate frequency (IF) amplifier circuit.

CONSTITUTION: An IF signal given to an IF signal input terminal 13 is amplified by a TR Q<sub>2</sub> and the result is outputted to an IF signal output terminal 14. A coil L<sub>1</sub> exists between a collector of the TR Q<sub>2</sub> (point a) and a gate of a FET Q<sub>1</sub> and the coil L<sub>1</sub> at the side of the FET Q<sub>1</sub> is grounded via a capacitor C<sub>1</sub>. Thus, since the IF signal at the point (a) and the BS signal of the gate of the FET Q<sub>1</sub> are insulated in terms of high frequency, the RF amplification by the FET Q<sub>1</sub> and the IF amplification by the TR Q<sub>2</sub> are implemented independently without any interference. That is, the bias stabilizing TR suppressing the fluctuation of the drain circuit of the RF amplifier FET is employed to constitute the IF amplifier circuit. Thus, number of components is reduced and the BS converter with small size and low cost is obtained.

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